Having thus described the preferred embodiment, the invention is now claimed to be:

1. A package mounting integrated circuit chips onto a circuit board comprising:

an integrated circuit chip having a surface array of input/output pads on one side thereof which array forms a footprint;

a chip carrier formed of an organic glass filled epoxy dielectric material having first and second opposite surfaces;

said chip carrier having a coefficient of thermal expansion of at least 17×10^{-6} ppm/c°;

a first set of bonding pads formed on said first surface of the chip carrier and arranged in an array corresponding with the chip footprint;

a pattern of conductors on said chip carrier connected to accommodate said input/output pads;

a first set of solder connections interconnecting the input/output pads on the chip to said first set of bonding pads on the chip carrier;

an encapsulation material encapsulating said first set of solder connections;

a second set of bonding pads formed on the second surface of the chip carrier arranged in an array;

electrically conducting vias extend through the chip carrier connecting said first set of bonding pads to the second set of bonding pads;

a circuit board formed of an organic material having a coefficient of thermal expansion similar to the chip carrier;

a set of electrical connection sites formed on said circuit board and arranged in a pattern corresponding to the pattern of the array of the second bonding pads on said chip carrier;

a second set of solder connections interconnecting the pads of said second set of bonding pads on the chip carrier to the connection sites on the circuit board; and

wiring on said circuit board connected to said second set of bonding pads.

2. The package of claim 1 wherein said chip carrier and said circuit board are formed of the same material.

3. The package as defined in claim 1 wherein said first set of solder connections is formed of a higher melting point solder than said second set of solder connections.

4. The package as defined in claim 1 further characterized by first bonding pads being more closely spaced to each other than said second bonding pads.

5. The package as defined in claim 1 wherein the thermal coefficient of expansions of the material of the chip carrier and the material of the circuit board do not differ by more than about 20%.

6. The package as defined in claim 1 wherein the thickness of the conductors on said chip carrier is thinner than the wires of the wiring on the circuit board.

7. A method of mounting integrated circuit chips onto a circuit board comprising the steps of:

providing an integrated circuit chip having a surface array of input/output pads on one side thereof which array forms a footprint;

providing a chip carrier formed of an organic glass filled epoxy dielectric material having first and second opposite surfaces;

said chip carrier having a coefficient of thermal expansion of at least 17×10^{-6} ppm/c°;

forming a first set of bonding pads on said first surface of the chip carrier arranged in an array corresponding with the chip footprint;

providing a pattern of conductors on said chip carrier connected to accommodate said input/output pads;

forming a first set of solder connections between the input/output pads on the chip and said first set of bonding pads on the chip carrier;

an encapsulation material encapsulating said first set of solder connections;

forming a second set of bonding pads on the second surface of the chip carrier arranged in an array;

forming electrically conducting vias through the chip carrier to connect said first set of bonding pads to the second set of bonding pads;

providing a circuit board formed of an organic material having a coefficient of thermal expansion similar to the chip carrier;

forming a set of electrical connection sites on said circuit board arranged in a pattern corresponding to the pattern of the array of the second bonding pads on said chip carrier;

forming a second set of solder connections between the pads of said second set of bonding pads on the chip carrier and the connection sites on the circuit board; and

forming wiring on said circuit board connected to said second set of bonding pads.

8. The method of claim **7** wherein said chip carrier and said circuit board are formed of the same material.

9. The method as defined in claim **7** wherein said first set of solder connections is formed of a higher melting point solder than said second set of solder connections.

10. The method as defined in claim **7** further characterized by first bonding pads being more closely spaced to each other than said second bonding pads.

11. The method as defined in claim **7** wherein the thermal coefficient of expansions of the material of the chip carrier and the material of the circuit board do not differ by more than about 20%.

12. The package as defined in claim **7** wherein the thickness of the conductors on said chip carrier is thinner than the wires of the wiring on the circuit board.

* * * * *

13. A package mounting integrated circuit chips onto a circuit board comprising:

an integrated circuit chip having a surface array of input/output pads on one side thereof which array forms a footprint;

a chip carrier formed of an organic dielectric material and having first and second opposite surfaces;

said chip carrier having a coefficient of thermal expansion of at least about 15×10^{-6} ppm/C°;

a first set of bonding pads formed on said first surface of the chip carrier and arranged in an array corresponding with the chip footprint;

a pattern of conductors on said chip carrier connected to accommodate said input/output pads;

a first set of solder connections interconnecting the input/output pads on the chip to said first set of bonding pads on the chip carrier;

an encapsulation material encapsulating said first set of solder connections;

a second set of bonding pads formed on the second surface of the chip carrier arranged in an array;

electrically conducting vias extend through the chip carrier connecting said first set of bonding pads to the second set of bonding pads;

a circuit board formed of an organic material having a coefficient of thermal expansion similar to the chip carrier;

a set of electrical connection sites formed on said circuit board and arranged in a pattern corresponding to the pattern of the array of the second bonding pads on said chip carrier;

a second set of solder connections interconnecting the pads of said second set of bonding pads on the chip carrier to the connection sites on the circuit board; and

wiring on said circuit board connected to said second set of bonding pads.

14. A package according to claim 13 wherein said chip carrier has a coefficient of thermal expansion of at least about 16×10^{-6} ppm/C°.

15. A package according to claim 13 wherein said chip carrier is formed of a glass filled epoxy.

16. A package mounting integrated circuit chips onto an organic dielectric circuit board having a coefficient of thermal expansion of at least about 15×10^{-6} ppm/C°, comprising:

an integrated circuit chip having a surface array of input/output pads on one side thereof which array forms a footprint;

a chip carrier formed of an organic dielectric material [formed of an organic dielectric material] having a coefficient of thermal expansion similar to the chip [carrier] and having first and second opposite surfaces;

a first set of bonding pads formed on said first surface of the chip carrier and arranged in an array corresponding with the chip footprint;

a pattern of conductors on said chip carrier connected to accommodate said input/output pads;

a first set of solder connections interconnecting the input/output pads on the chip to said first set of bonding pads on the chip carrier;

an encapsulation material encapsulating said first set of solder connections;

a second set of bonding pads formed on the second surface of the chip carrier arranged in an array;

electrically conducting vias extend through the chip carrier connecting said first set of bonding pads to the second set of bonding pads;

a set of electrical connection sites formed on said circuit board and arranged in a pattern corresponding to the pattern of the array of the second bonding pads on said chip carrier;

a second set of solder connections interconnecting the pads of said second set of bonding pads on the chip carrier to the connection sites on the circuit board; and

wiring on said circuit board connected to said second set of bonding pads.

17. A package according to claim 16 wherein the thermal coefficient of expansions of the material of the chip carrier and the material of the circuit board do not differ by more than about 20%.

18. A package according to claim 16 wherein said chip carrier and said circuit board are formed of the same material.

19. A package according to claim 16 wherein said chip carrier is formed of a glass filled epoxy.

20. A package according to claim 16 wherein said chip carrier has a coefficient of thermal expansion of at least about 16×10^{-6} ppm/C°.

21. A package mounting integrated circuit chips onto a circuit board comprising:

an integrated circuit chip having a surface array of input/output pads on one side thereof which array forms a footprint;

a chip carrier formed of an organic dielectric material having first and second opposite surfaces;

a first set of bonding pads formed on said first surface of the chip carrier and arranged in an array corresponding with the chip footprint;

a pattern of conductors on said chip carrier connected to accommodate said input/output pads;

a first set of solder connections interconnecting the input/output pads on the chip to said first set of bonding pads on the chip carrier;

an encapsulation material encapsulating said first set of solder connections;

a second set of bonding pads formed on the second surface of the chip carrier arranged in an array;

electrically conducting vias extend through the chip carrier connecting said first set of bonding pads to the second set of bonding pads;

a circuit board formed of an organic material having a coefficient of thermal expansion similar to the chip carrier;

a set of electrical connection sites formed on said circuit board and arranged in a pattern corresponding to the pattern of the array of the second bonding pads on said chip carrier;

a second set of solder connections interconnecting the pads of said second set of bonding pads on the chip carrier to the connection sites on the circuit board; and

wiring on said circuit board connected to said second set of bonding pads.

22. A package according to claim 21 wherein the thermal coefficient of expansions of the material of the chip carrier and the material of the circuit board do not differ by more than about 20%.

23. The package of claim 21 wherein said chip carrier and said circuit board are formed of the same material.

24. A package according to claim 21 wherein said chip carrier is formed of a glass filled epoxy.

25. A package according to claim 21 wherein said chip carrier is formed of a polyimide.

~~26. A method of mounting integrated circuit chips onto a~~ circuit board comprising the steps of:

providing an integrated circuit chip having a surface array of input/output pads on one side thereof which array forms a footprint;

providing a chip carrier formed of an organic ~~dielectric material having~~ a coefficient of thermal expansion of at least about 15×10^{-6} ppm/c°, and having first and second ~~opposite surfaces;~~

forming a first set of bonding pads on said first surface of the chip carrier arranged in an array corresponding with the chip footprint;

providing a pattern of conductors on said chip carrier connected to accommodate said input/output pads;

forming a first set of solder connections between the input/output pads on the chip and said first set of bonding pads on the chip carrier;

encapsulating said first set of solder connections;

forming a second set of bonding pads on the second surface of the chip carrier arranged in an array;

forming electrically conducting vias through the chip carrier to connect said first set of bonding pads to the second set of bonding pads;

providing a circuit board formed of an organic material having a coefficient of thermal expansion similar to the chip carrier;

forming a set of electrical connection sites on said circuit board arranged in a pattern corresponding to the pattern of the array of the second bonding pads on said chip carrier;

forming a second set of solder connections between the pads of said second set of bonding pads on the chip carrier and the connection sites on the circuit board; and

forming wiring on said circuit board connected to said second set of bonding pads.

27. The method of claim 26 wherein said chip carrier and said circuit board are formed of the same material.

28. The method as defined in claim 26 wherein the thermal coefficient of expansions of the material of the chip carrier and the material of the circuit board do not differ by more than about 20%.

29. A method of mounting integrated circuit chips onto an organic dielectric circuit board having a coefficient of thermal expansion of at least about 15×10^{-6} ppm/C°, comprising the steps of:

providing an integrated circuit chip having a surface array of input/output pads on one side thereof which array forms a footprint;

providing a chip carrier formed of an organic dielectric material having a coefficient of thermal expansion similar to the circuit board, said chip carrier having first and second opposite surfaces;

forming a first set of bonding pads on said first surface of the chip carrier arranged in an array corresponding with the chip footprint;

providing a pattern of conductors on said chip carrier connected to accommodate said input/output pads;

forming a first set of solder connections between the input/output pads on the chip and said first set of bonding pads on the chip carrier;

encapsulating said first set of solder connections with an encapsulation material;

forming a second set of bonding pads on the second surface of the chip carrier arranged in an array;

forming electrically conducting vias through the chip carrier to connect said first set of bonding pads to the second set of bonding pads;

forming a set of electrical connection sites on said circuit board arranged in a pattern corresponding to the pattern of the array of the second bonding pads on said chip carrier;

forming a second set of solder connections between the pads of said second set of bonding pads on the chip carrier and the connection sites on the circuit board; and

forming wiring on said circuit board connected to said second set of bonding pads.

30. A method according to claim 29 wherein said chip carrier has a coefficient of thermal expansion of at least about ~~16×10^{-6}~~ ppm/C°.

31. A method according to claim 29 wherein said chip carrier has a coefficient of thermal expansion of at least about 17×10^{-6} ppm/C°.

32. A method according to claim 29 wherein said chip carrier is formed of a glass filled epoxy.

33. A method according to claim 29 wherein said chip carrier is formed of a polyimide.

34. A method of mounting integrated circuit chips onto a circuit board comprising:

providing an integrated circuit chip having a surface array of input/output pads on one side thereof which array forms a footprint;

providing a chip carrier formed of an organic dielectric material having first and second opposite surfaces;

forming a first set of bonding pads formed on said first surface of the chip carrier and arranged in an array corresponding with the chip footprint;

providing a pattern of conductors on said chip carrier connected to accommodate said input/output pads;

forming a first set of solder connections interconnecting the input/output pads on the chip to said first set of bonding pads on the chip carrier;

encapsulating said first set of solder connections;

forming a second set of bonding pads formed on the second surface of the chip carrier arranged in an array;

forming electrically conducting vias extend through the chip carrier connecting said first set of bonding pads to the second set of bonding pads;

providing a circuit board formed of an organic material having a coefficient of thermal expansion similar to the chip carrier;

forming a set of electrical connection sites on said circuit board and arranged in a pattern corresponding to the pattern of the array of the second bonding pads on said chip carrier;

forming a second set of solder connections interconnecting the pads of said second set of bonding pads on the chip carrier to the connection sites on the circuit board; and

forming wiring on said circuit board connected to said second set of bonding pads.